Standard Mode

– without I^2C

In standard mode, sample rates from 48 kHz to 32 kHz are handled without I^2C control automatically. The setting for this range is the default setting.

– with I^2C

Sample rates below 32 kHz require an I^2C control to set the PLL divider. This ensures that even at low sample rates, the DAC 3550A runs at a high clock rate. This avoids audible effects due to the noise-shaping technique of the DAC 3550A. Sample rate range is continuous from 8 to 50 kHz. The I^2C setting of low sample rates must follow.

An additional mode allows automatic sample rate detection. In this case, the clock oscillator is required and must run at frequencies between 13.3 MHz to 17 MHz. This mode, however, does not support continuous sample rates. Only the following sample rates are allowed: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz.

The sample rate detection allows a tolerance of ±200 ppm at WSI.

If the oscillator is not used for automatic sample rate detection, it can be used as a general-purpose clock for the application. The frequency range in this case is 10 MHz to 25 MHz.

MPEG Mode

This mode should be used in conjunction with MAS 3507D in MPEG player applications. In this case a 14.725 MHz signal is needed to provide a clock for the MAS 3507D and to allow an automatic sample rate detection in the DAC 3550A. All MPEG sample rates from 8 to 48 kHz can be detected. The internal processing and the DAC itself are automatically adjusted to keep constant performance throughout the entire range. I^2C control for sample rate adjustment is not needed in this case. Register SR_REG[0:2] is locked to SRC_A.

The MPEG sample rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz.

As in standard mode, the sample rate detection allows a tolerance of ±200 ppm at WSI.

Subaddressing is not possible in MPEG mode; this means, in multi-DAC systems, only one DAC 3550A can run in MPEG mode.

Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T_A	Ambient Temperature range 1)		0		70	°C
V_{SUPA1}	Analog Audio Supply Voltage	AVDD0/1	3.0 2)	3.3	5.5	V
V_{SUPD}	Digital Audio Supply Voltage	VDD	2.7	3.3	5.5	V
Relative Supply Voltages						
V_{SUPA}	Analog Audio Supply Voltage in relation to the Digital Supply Voltage	AVDD0/1	V_{SUPD}–0.25 V		5.5 V	V
Analog Reference						
C_{AGNDC1}	Analog Reference Capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Analog Reference Capacitor	AGNDC		10		nF
Analog Audio Inputs						
V_{AI}	Analog Input Voltage AC, SEL_53V = 0	AUXnL/R 3)		0.35	0.7	V_{rms}
V_{AI}	Analog Input Voltage AC, SEL_53V = 0	AUXnL/R 3)		0.525	1.05	V_{rms}

DAC3550A
Stereo Audio DAC

Manufacturer

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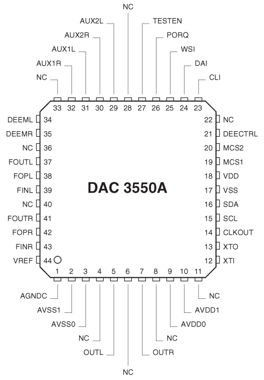
Example Application

MP3 Player, *Elektor Electronics* July/August 2000.

Description

The DAC 3550A is a single-chip, high-precision, dual digital-to-analog converter designed for audio applications. The employed conversion technique is based on oversampling with noise-shaping.

With MICRONAS INTERMETALL's unique multibit sigma-delta technique, less sensitivity to clock jitter, high linearity, and a superior S/N ratio has been achieved. The DAC 3550A is controlled via I^2C bus. Digital audio input data is received by a versatile I^2S interface. The analog back-end consists of internal analog filters and op amps for cost-effective additional external sound processing. The DAC 3550A provides line-out, headphone/speaker amplifiers, and volume control. Moreover, mixing additional analog audio sources to the D/A-converted signal is supported. The DAC 3550A is designed for all kinds of applications in the audio and multimedia field, such as: MPEG players, CD players, DVD players, CD-ROM players, etc. The DAC 3550A ideally complements the MPEG 1/2 layer 2/3 audio decoder MAS 3507D. **No crystal required for standard applications with sample rates from 32 to 48 kHz.** Crystal required only for automatic sample rate detection below 32 kHz, MPEG mode, and use of clock output CLKOUT.



44-pin PMQFP package.

Main Features

- no master main input clock required
- integrated stereo headphone amplifier and mono speaker amplifier
- SNR of 103dBA
- I^2C bus, I^2S bus
- internal clock oscillator
- full-feature mode by I^2C control (three selectable subaddresses)
- reduced feature mode for non-I^2C applications
- continuous sample rates from 8 kHz to 50 kHz
- analog de-emphasis for 44.1 kHz
- analog volume and balance: +18 to –75 dB and mute
- oversampling and multibit noise-shaping technique
- THD better than 0.01 %
- two additional analog stereo inputs (AUX) with source selection and mixing
- supply range: 2.7 V to 5.5 V
- low-power mode
- additional line-out
- on-chip op amps for cost-effective external analog sound processing

Pin Descriptions

1. Power Supply Pins

The DAC 3550A combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

VDD (18), VSS (17)

The VDD and VSS power supply pair are connected internally with all digital parts of the DAC 3550**A**.

AVDD0 (9), AVSS0 (3)

AVDD0 and AVSS0 are separate power supply pins that are exclusively used for the on-chip headphone/loudspeaker amplifiers.

AVDD1 (10), AVSS1 (2)

The AVDD1 and AVSS1 pins supply the analog audio processing parts, except for the headphone/loud-speaker amplifiers.

2. Analog Audio Pins

AGNDC (1)

Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against VREF with a 3.3 µF capacitor.

Note: The pin has a typical DC-level of 1.5/2.25 V. It can be used as reference input for external op amps when no current load is applied.

VREF (44)

Reference ground for the internal band-gap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the DAC 3550A.

AUX1L (31), AUX1R (32), AUX2L (29), AUX2R (30)

The AUX pins provide two analog stereo inputs. Auxiliary input signals, e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected with these inputs. The input signals have to be connected by capacitive coupling .

FOUTL (37), FOPL (38), FINL (39), FOUTR (41), FOPR (42), FINR (43)

Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R-pins are directly connected with the inverting inputs of the filter op amps. The FINL/R pins are connected with the outputs of the op amps. The driving capability of the FOUTL/R pins is not sufficient for standard line output signals. Only the FINL/R pins are suitable for line output.

OUTL (5), OUTR (7)

The OUTL/R pins are connected to the internal output amplifiers. They can be used for either stereo head-phones or a mono loudspeaker. The signal of the right channel amplifier can be inverted for mono loud-speaker operation.

Caution: A short circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

3. Oscillator and Clock Pins

XTI (12), XTO (13)

The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Both pins should be directly connected to the crystal and two ground-connected capacitors.

CLKOUT (14)

The CLKOUT pin provides a buffered output of the crystal oscillator.

Caution: Power dissipation limit may be exceeded in case of short to VSS or VDD.

CLI (23), DAI (24), WSI (25)

These three pins are inputs for the digital audio data DAI, frame indication signal WSI, and bit clock CLI. The digital audio data is transmitted in an I^2S-compatible format. Audio word lengths of 16 and 32 bits are supported, as well as SONY and Philips I^2S protocol.

SCL (15), SDA (16)

SCL (serial clock) and SDA (serial data) provide the connection to the serial control interface (I^2C).

4. Other Pins

TESTEN (27)

Test enable. This pin is for test purposes only and must always be connected to VSS.

PORQ (26)

This pin may be used to reset the chip. If not used, this pin must be connected to VDD.

DEEML (34), DEEMR (35)

These pins connect an external analog de-emphasis network to the signal path in the analog back-end. This connection can be switched on and off by an internal switch which is controlled either by I^2C or the DEECTRL pin.

DEECTRL (21)

If no I^2C control is used, de-emphasis can be switched on and off with this pin.

MCS1 (19), MCS2 (20)

Mode select pins to select MPEG, Standard Mode, and I^2C subaddress.

Operation Modes

MCS1	MCS2	Mode	Sub-address	Default Sample Rate
0	0	Standard	ADR0	32-48 kHz
0	1	Standard	ADR1	32-48 kHz
1	0	Standard	ADR2	32-48 kHz
1	1	MPEG	ADR3	Automatic

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Filter Input and Output						
Z_{AFLO}	Analog Filter Load Output 4)	FOUTL/R	7.5			kΩ
					6.0	pF
ZAFLI	Analog Filter Load Input 4)	FINL/R	5.0			kΩ
					7.5	pF
Analog Audio Output						
Z_{LO}	Audio Line Output 5) (680Ω series resistor required)	FINL/R	10			kΩ
					1.0	nF
Z_{AOL_HP}	Analog Output Load HP (47Ω series resistor required)	OUTL/R		32		Ω
				400		pF
Z_{AOL_SP}	Analog Output Load SP (bridged)	OUTL/R		32		Ω
				50		pF
	Analog Output Load SP (stereo)			16		Ω
				100		pF
I^2C Input						
f_{I2C1}	I^2C Clock Frequency, I^2S active	SCL		400		kHz
f_{I2C2}	I^2C Clock Frequency, I^2S inactive			100		kHz
Digital Inputs						
V_{IH}	Input High Voltage	CLI, WSI, DAI, PORQ, SCL, SDA	0.5 ×VDD			V
V_{IL}	Input Low Voltage				0.2 ×VDD	V
Quartz Characteristics						
Fp	Load Resonance frequency at $C_l = 20pF$		13.3	14.725	17	MHz
R_{EQ}	Equivalent Series Resistance			12	30	Ω
C_0	Shunt (parallel) Capacitance			3	5	pF
Load at CLKOUT Output						
C_{load}	Capacitance	CLKOUT	0		50	pF

1) =standard temperature range, DAC 3550A tested in extended temperature range on request
2) typically operable down to 2.7 V, without loss in performance
3) n = 1 or 2
4) Please refer to Section 4.2. “Recommended Low-Pass Filters for Analog Outputs” on page 25 of Micronas datasheets.
5) Please refer to Section 4.1. “Line Output Details” on page 25 of Micronas datasheets.